FAME RE-ALLOCATION OPTIONS

FAME RE-ALLOCATION Options - Summary.

Option	Description	Greatest Delta	Feasibility
A	Ground Image Processing	No image processing at Instrument but processor remains.	Task shift only, No significant cost savings.
B	Ground Instrument Control	No processing at Instrument	Not Feasible Uplink > 2K
C	Bus Image Processing	No image processing at Instrument but processor remains.	Task shift only, No significant cost savings. (Possible increase.)
D	Bus Instrument Control	No processing at Instrument, No processor.	Significant cost savings.
E	Bus Instrument Control, Ground Image Processing	No processing at Instrument, No processor.	Significant cost savings.
F	Bus Instrument	No processing at	Significant cost

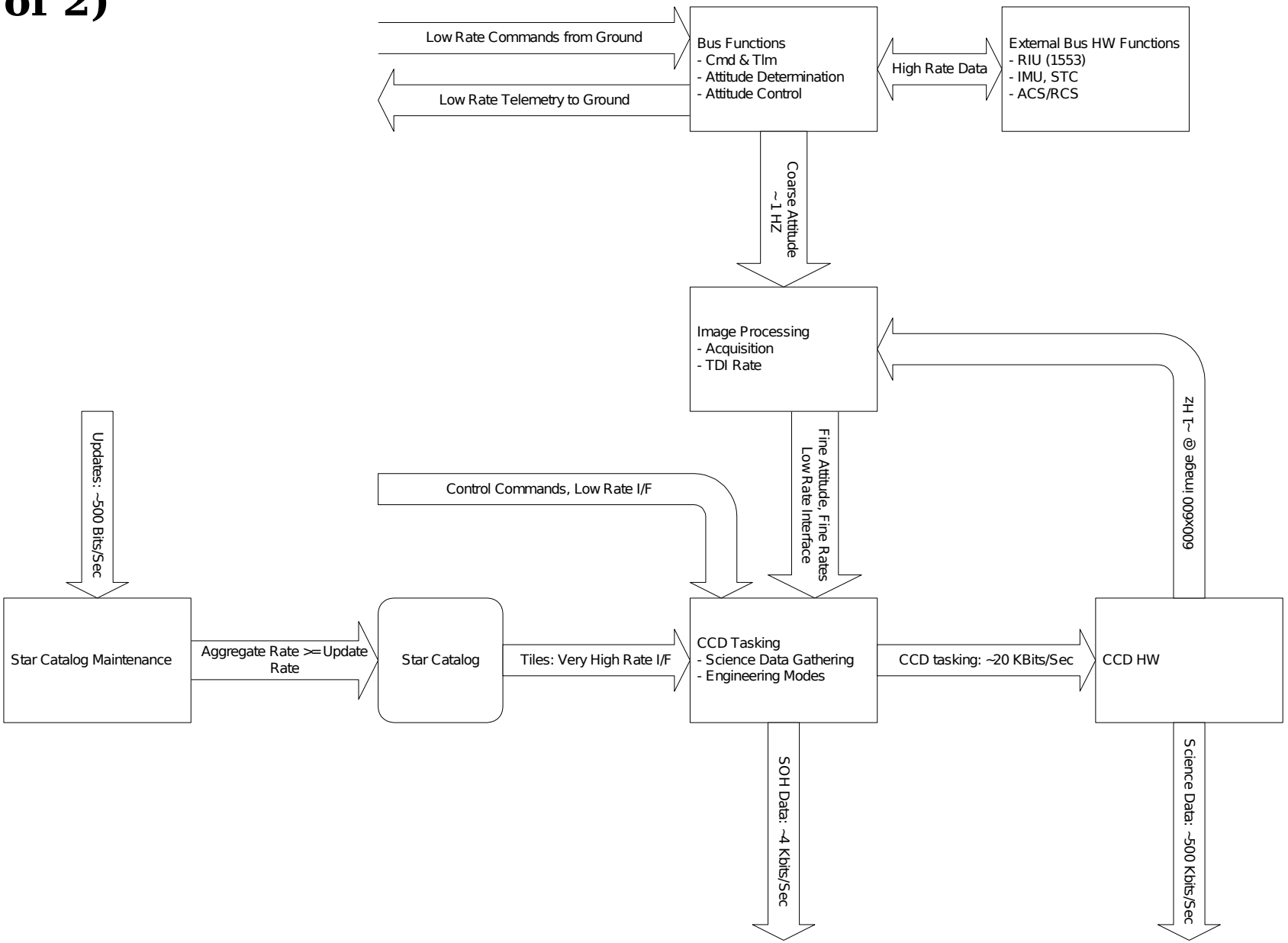
FAME High Level Data Processing and Data Interfaces (1 of 2)

- The processing outlined in the diagrams is intended to represent all current functions allocated to the FAME Bus and Instrument. The partitioning was selected to show potential reallocations of these functions between the ground based processing, Bus Processor (FSC) and the Instrument Processor.

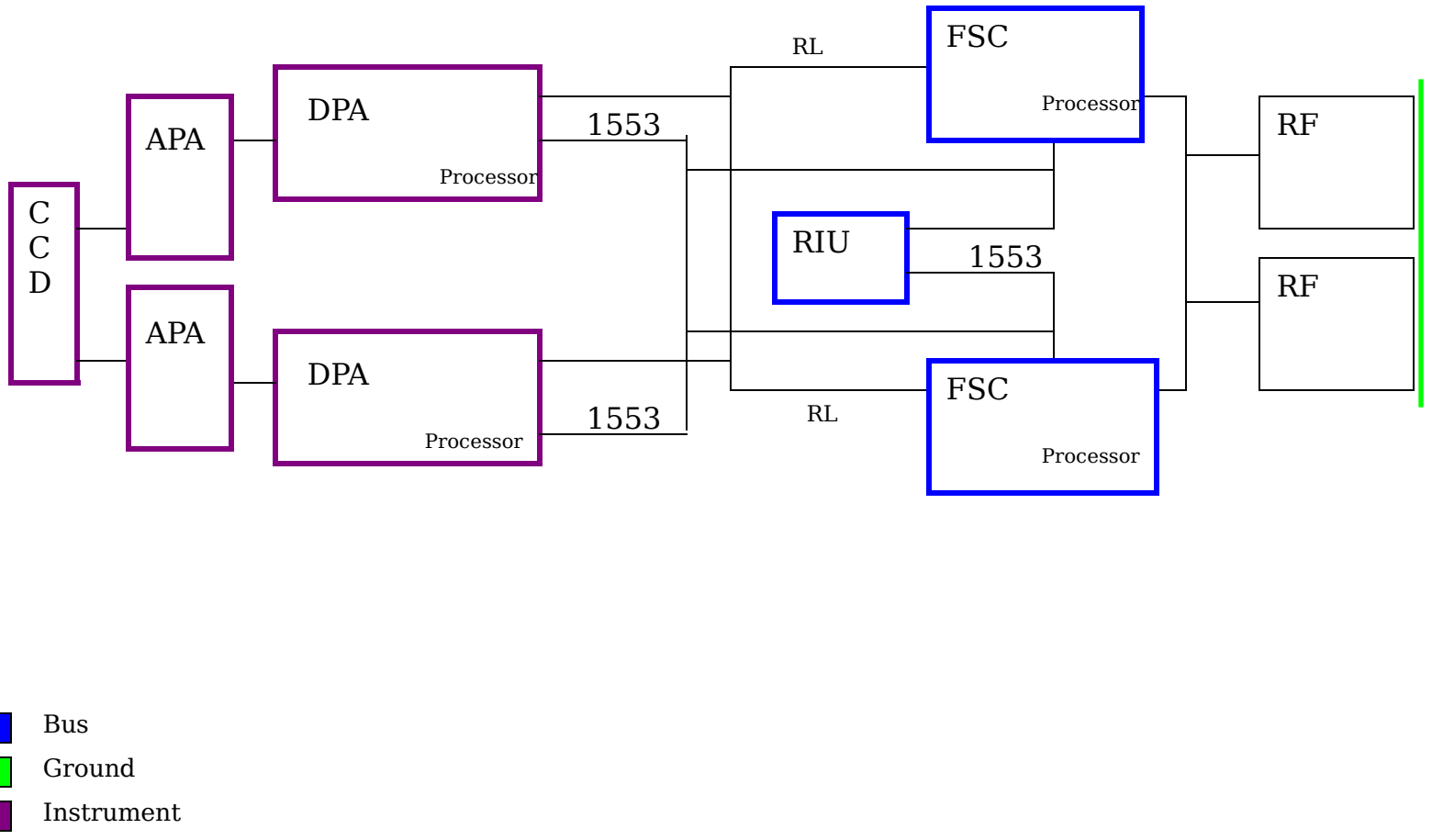
- The interfaces between these functions provide a summary description of the data and rough order of the bandwidth requirements. These interfaces are shown to help assess the viability of function reallocation.

- Note: The diagrams show the Science Data interface has been allocated directly to the CCD HW "function". This is a delta from the Instrument PDR baseline. This approach is being considered by LM ATC and is a recommended approach.

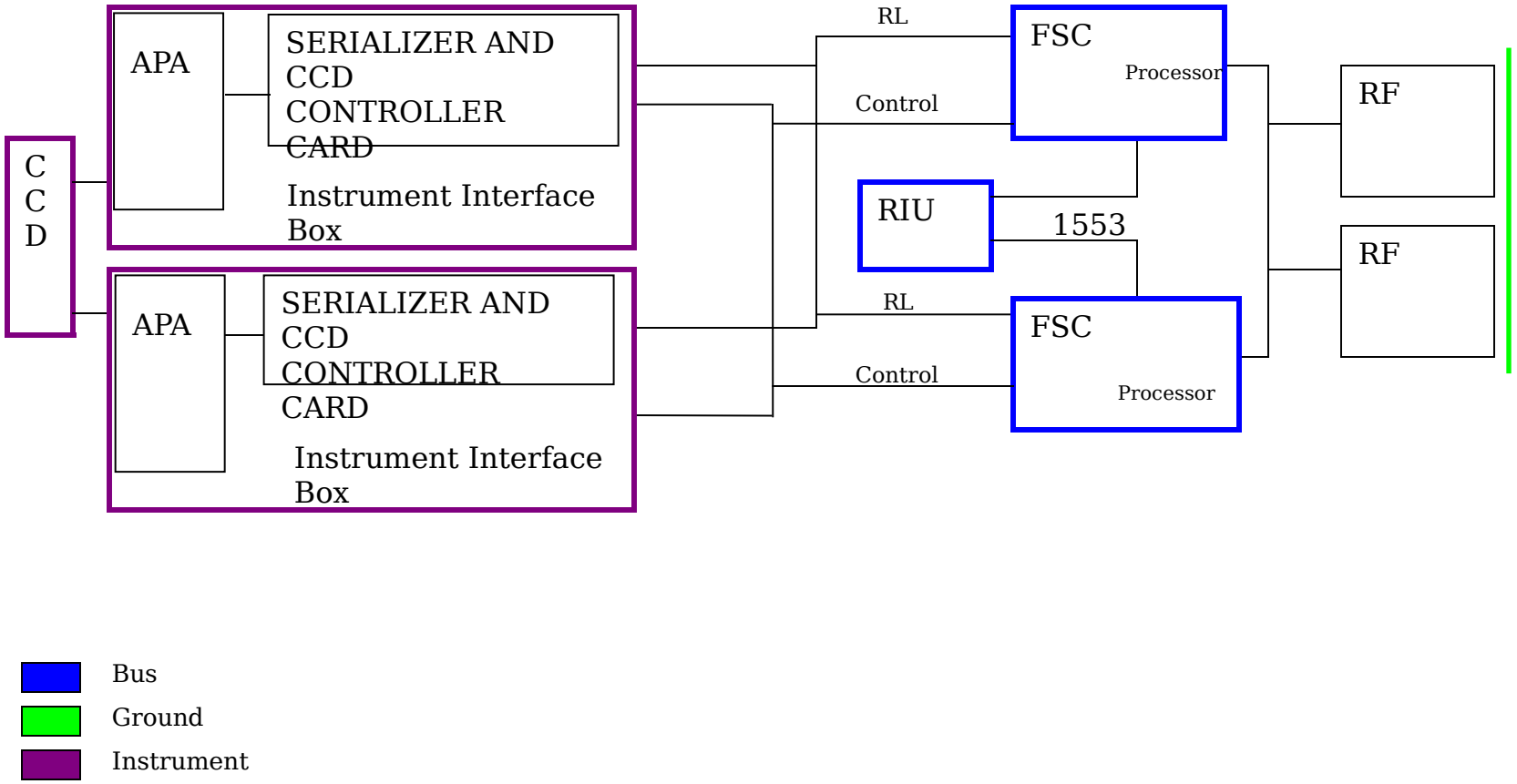
FAME High Level Data Processing and Data Interfaces (2 of 2)



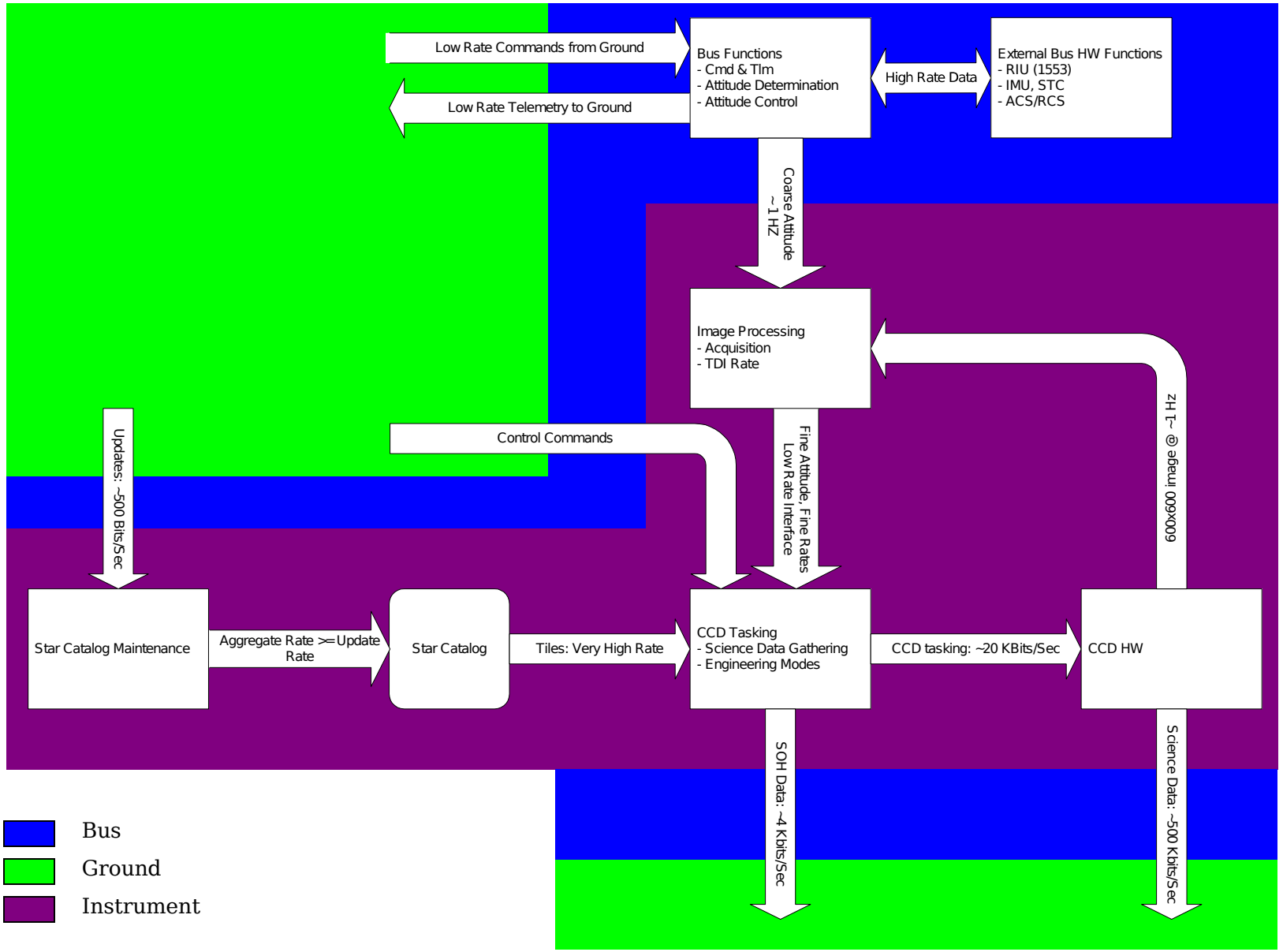
FAME - Baseline Hardware Configuration
- Representative of Options A and C



FAME - Optional Hardware Configuration - Representative of Options B, D, E and F.



FAME Baseline Processing and Data Interface Allocation

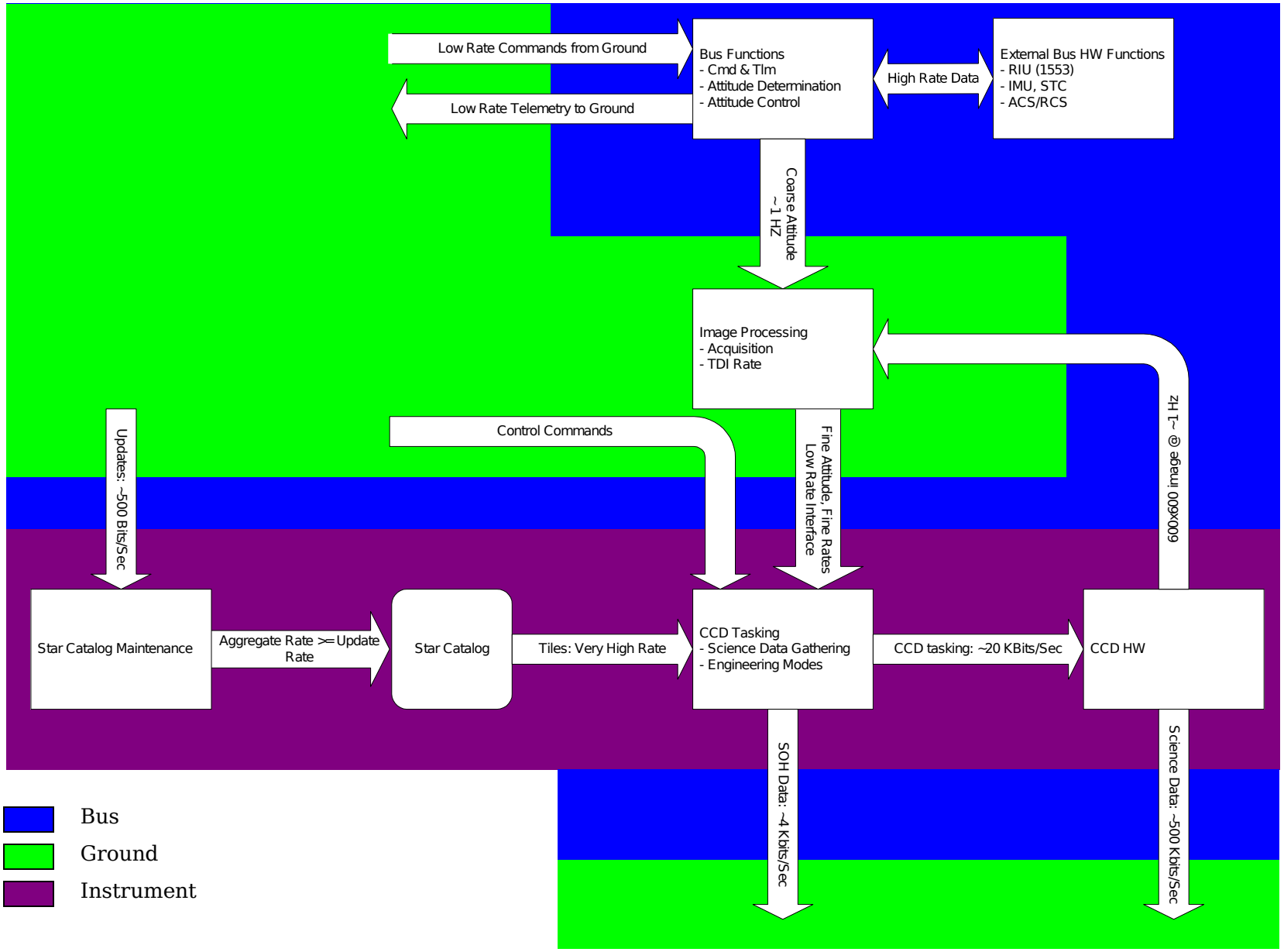


Re-allocation A: Ground Image Processing (1 of 2)

Re-Allocation Approach A	Baseline	Delta	Delta Cost
Processing			
Image Processing	Instrument Processor	Ground Processing	Decrease
CCD Tasking	Instrument Processor	-	-
Star Catalog Maintenance	Instrument Processor	-	-
Interfaces			
Coarse Attitude/Rates	Bus/Instrument	Bus/Ground (existing)	No Change
Tracking Image	Instrument Internal	Instrument/Ground (new)	Increase
Fine Attitude/Rates	Instrument Internal	Ground/Bus/Instrument (new)	Minor Increase
Star Catalog Updates	Ground/Bus/Instrument	-	-
Instrument Control	Ground/Bus/Instrument	-	-
CCD Tasking	Instrument Internal	-	-
Hardware (retain baseline configuration)			
Instrument Processor	2 x RHC-3001	-	-
Instrument 1553 I/F	2 x Harris 1553 Module	-	-
Flash Memory	1 x 1 Gbyte (shared)	-	-
Instrument CCD Control I/F	Instrument Internal	-	-
Bus CCD Control I/F	Not Required	-	-
Instrument Processor Related Manufacturing, Integ & Test	Baseline	-	-
Instrument Weight	Baseline	-	-
Bus Processor Design, Manufacturing, Integ & Test	Baseline	-	-
Uplink Rate	2000 bps	-	-

- Risk Increase
  - Continuous ground processing w/low rate uplink required for science data collection (less autonomy)
- Risk Reduction
  - Lessens Instrument CPU processing requirements

Re-allocation A: Ground Image Processing (2 of 2)

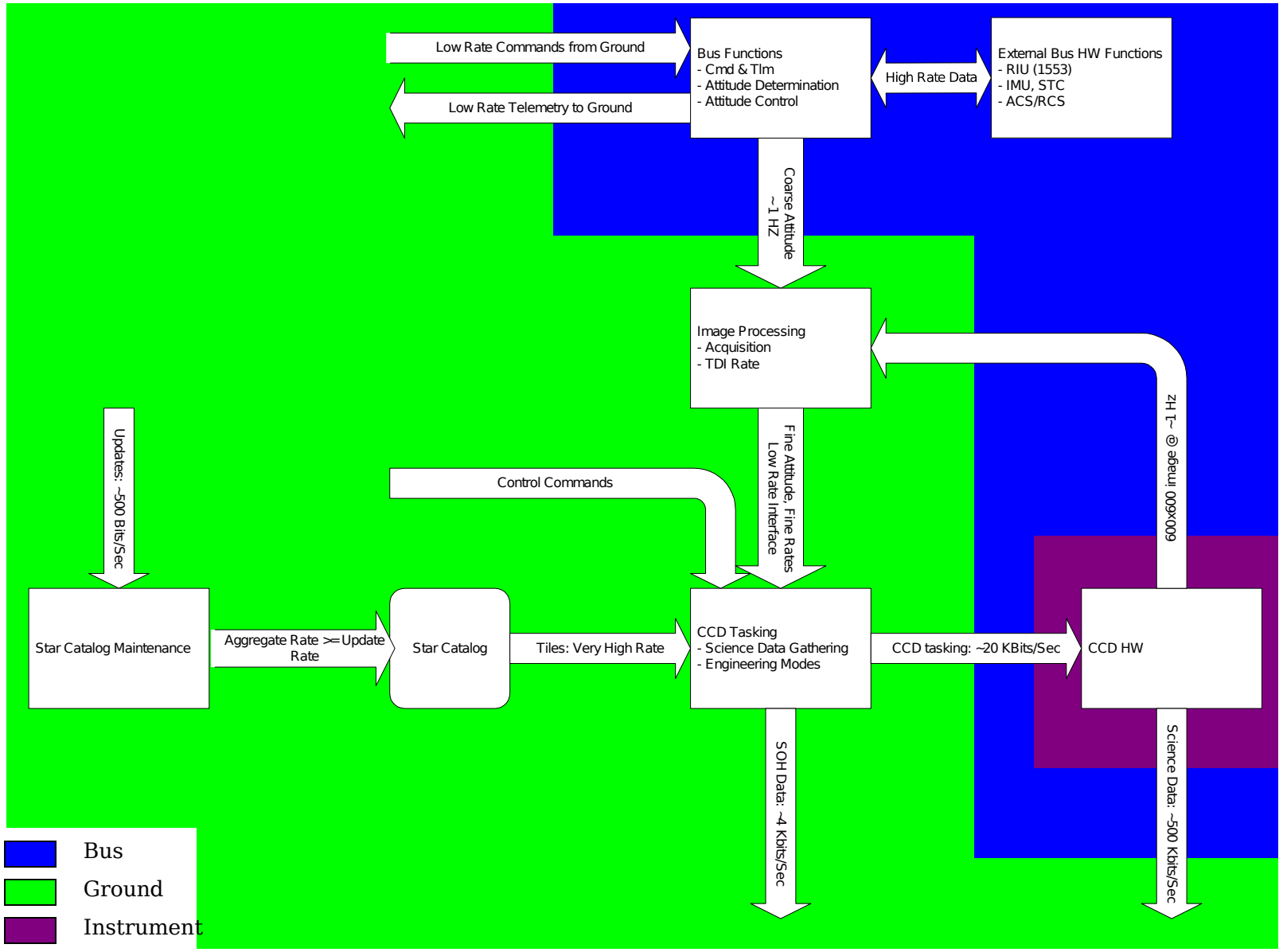


Re-allocation B: Ground Instrument Control (1 of 2)

Re-Allocation Approach B	Baseline	Delta	Delta Cost
Processing			
Image Processing	Instrument Processor	Ground Processing	Decrease
CCD Tasking	Instrument Processor	Ground Processing	Decrease
Star Catalog Maintenance	Instrument Processor	Ground Processing	Decrease
Interfaces			
Coarse Attitude/Rates	Bus/Instrument	Bus/Ground (existing)	No Change
Tracking Image	Instrument Internal	Instrument/Ground (new)	Increase
Fine Attitude/Rates	Instrument Internal	Ground Internal (New)	Minor Decrease
Star Catalog Updates	Ground/Bus/Instrument	Ground Internal (New)	Minor Decrease
Instrument Control	Ground/Bus/Instrument	Ground Internal (New)	Minor Decrease
CCD Tasking	Instrument Internal	Ground/Bus/Instrument (New)	Increase
Hardware (use optional hardware configuration)			
Instrument Processor	2 x RHC-3001	Not Needed	$500K Parts
Instrument 1553 I/F	2 x Harris 1553 Module	Not Needed	$200K Parts
Instrument Flash Memory	1 x 1 Gbyte (shared)	Not Needed	$100K Parts
Instrument CCD Control I/F	Instrument Internal	Not Needed	Offsetting Decrease
Bus CCD Control I/F	Not Required	Required	Offsetting Increase
Instrument Processor Related Manufacturing, Integ. & Test	Baseline	Significantly Reduced	Significant Decrease
Instrument Weight & Power	Baseline	Reduced	Decrease
Bus Processor Design, Manufacturing, Integ. & Test	Baseline	-	-
Uplink Rate	2,000 bps	~20,000 Bps	Increase

- Risk Increase
  - Continuous ground processing with continuous high rate uplink required for science data collection (no autonomy)
- Risk Reduction
  - Less flight HW & SW
  - Instrument processing constraints no longer a problem
  - Increase in reliability (I.e. less HW)

Re-allocation B: Ground Instrument Control (2 of 2)

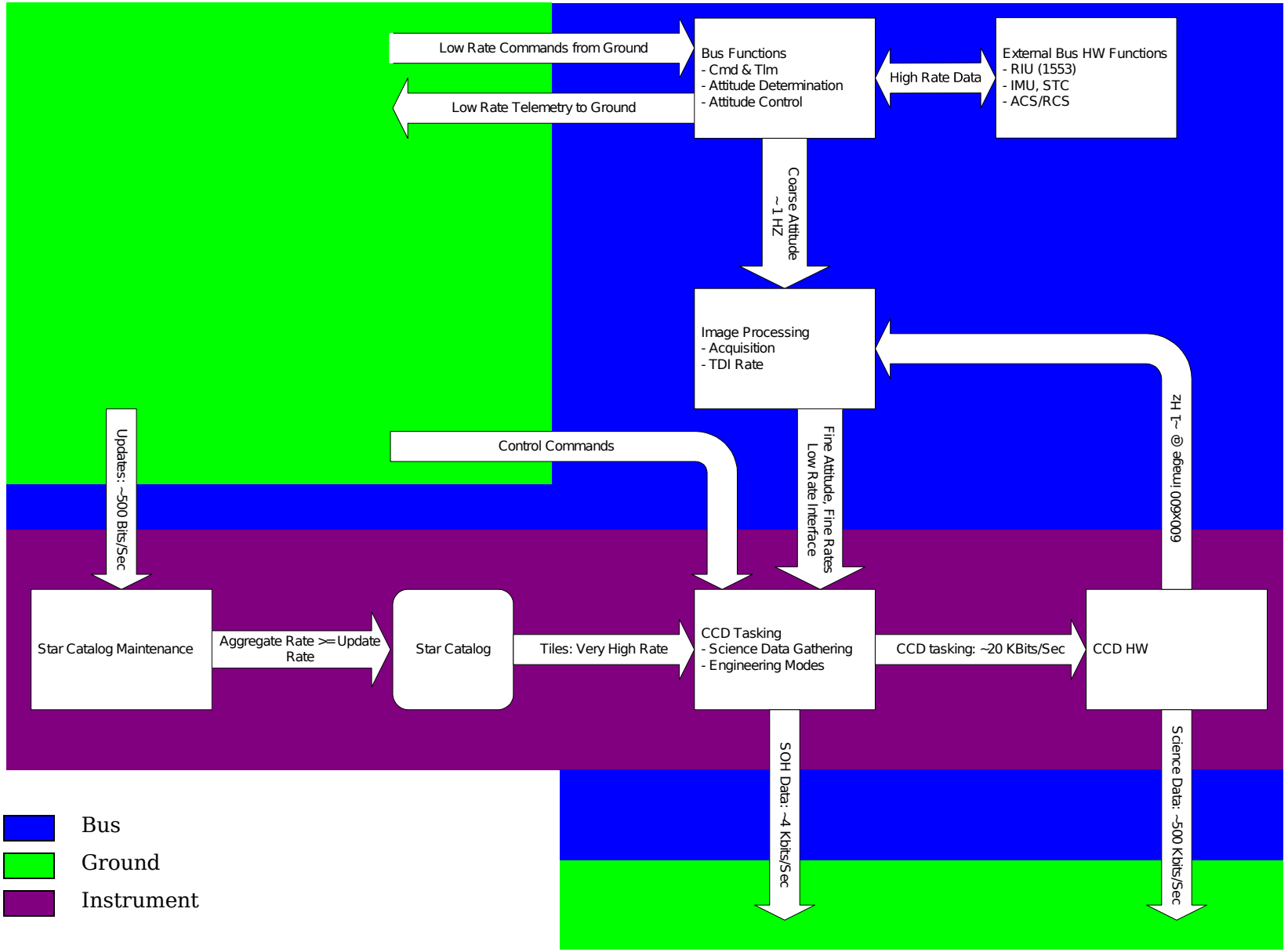


Re-allocation C: Bus Image Processing (1 of 2)

Re-Allocation Approach C	Baseline	Delta	Delta Cost
Processing			
Image Processing	Instrument Processor	Bus Processor	No Change
CCD Tasking	Instrument Processor	Ground Processing	-
Star Catalog Maintenance	Instrument Processor	Ground Processing	-
Interfaces			
Coarse Attitude/Rates	Bus/Instrument	Bus Internal (existing)	No Change
Tracking Image	Instrument Internal	Instrument/Bus (New)	Increase
Fine Attitude/Rates	Instrument Internal	Bus/Instrument (New)	Minor Increase
Star Catalog Updates	Ground/Bus/Instrument	-	-
Instrument Control	Ground/Bus/Instrument	-	-
CCD Tasking	Instrument Internal	-	-
Hardware (retain baseline configuration)			
Instrument Processor	2 x RHC-3001	-	-
Instrument 1553 I/F	2 x Harris 1553 Module	-	-
Instrument Flash Memory	1 x 1 Gbyte (shared)	-	-
Instrument CCD Control I/F	Instrument Internal	-	-
Bus CCD Control I/F	Not Required	-	-
Instrument Processor Related Manufacturing, Integ. & Test	Baseline	-	-
Instrument Weight	Baseline	-	-
Bus Processor Design, Manufacturing, Integ. & Test	Baseline	Potential Increase In Complexity (dependent on HW IF for images)	Increase
Uplink Rate	2,000 bps	-	-

- Risk Increase
  - No significant increase in risk
- Risk Reduction
  - Lessens Instrument CPU processing requirements

Re-allocation C: Bus Image Processing (2 of 2)

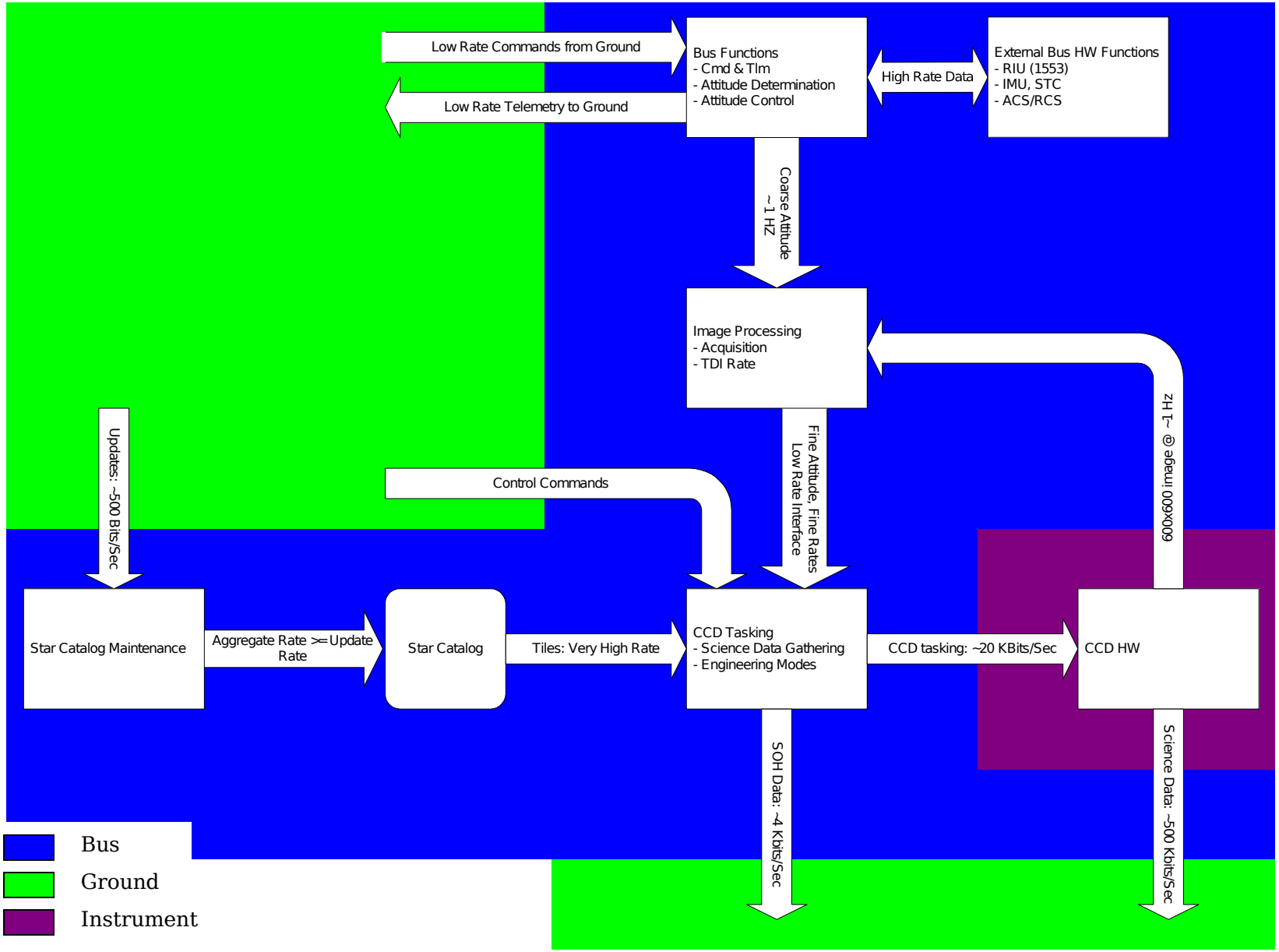


Re-allocation D: Bus Instrument Control (1 of 2)

Re-Allocation Approach D	Baseline	Delta	Delta Cost
Processing			
Image Processing	Instrument Processor	Bus Processor	No Change
CCD Tasking	Instrument Processor	Bus Processor	No Change
Star Catalog Maintenance	Instrument Processor	Bus Processor	No Change
Interfaces			
Coarse Attitude/Rates	Bus/Instrument	Bus Internal (Existing)	No Change
Tracking Image	Instrument Internal	Instrument/Bus (New)	Increase
Fine Attitude/Rates	Instrument Internal	Bus Internal (New)	No Change
Star Catalog Updates	Ground/Bus/Instrument	Ground/Bus (Existing)	No Change
Instrument Control	Ground/Bus/Instrument	Ground/Bus (Existing)	No Change
CCD Tasking	Instrument Internal	Bus/Instrument (New)	No Change
Hardware (use optional hardware configuration)			
Instrument Processor	2 x RHC-3001	Not Needed	$500K Parts
Instrument 1553 I/F	2 x Harris 1553 Module	Not Needed	$200K Parts
Instrument Flash Memory	1 x 1 Gbyte (shared)	Not Needed	$100K Parts
Instrument CCD Control I/F	Instrument Internal	Not Needed	Offsetting Decrease
Bus CCD Control I/F	Not Required	Required	Offsetting Increase
Instrument Processor Related Manufacturing, Integ. & Test	Baseline	Significantly Reduced	Significant Decrease
Instrument Weight	Baseline	Reduced	Decrease
Bus Processor Design, Manufacturing, Integ. & Test	Baseline	Increased Complexity (additional HW interfaces)	Increase
Uplink Rate	2,000 bps	-	-

- Risk Increase
  - Less processing bandwidth is available (one processor for both Instrument & Bus Functions instead of 2)
- Risk Reduction
  - Less flight HW
  - Instrument/Bus 1553 I/F not required
  - Increase in reliability (I.e. less HW)

Re-allocation D: Bus Instrument Control (2 of 2)

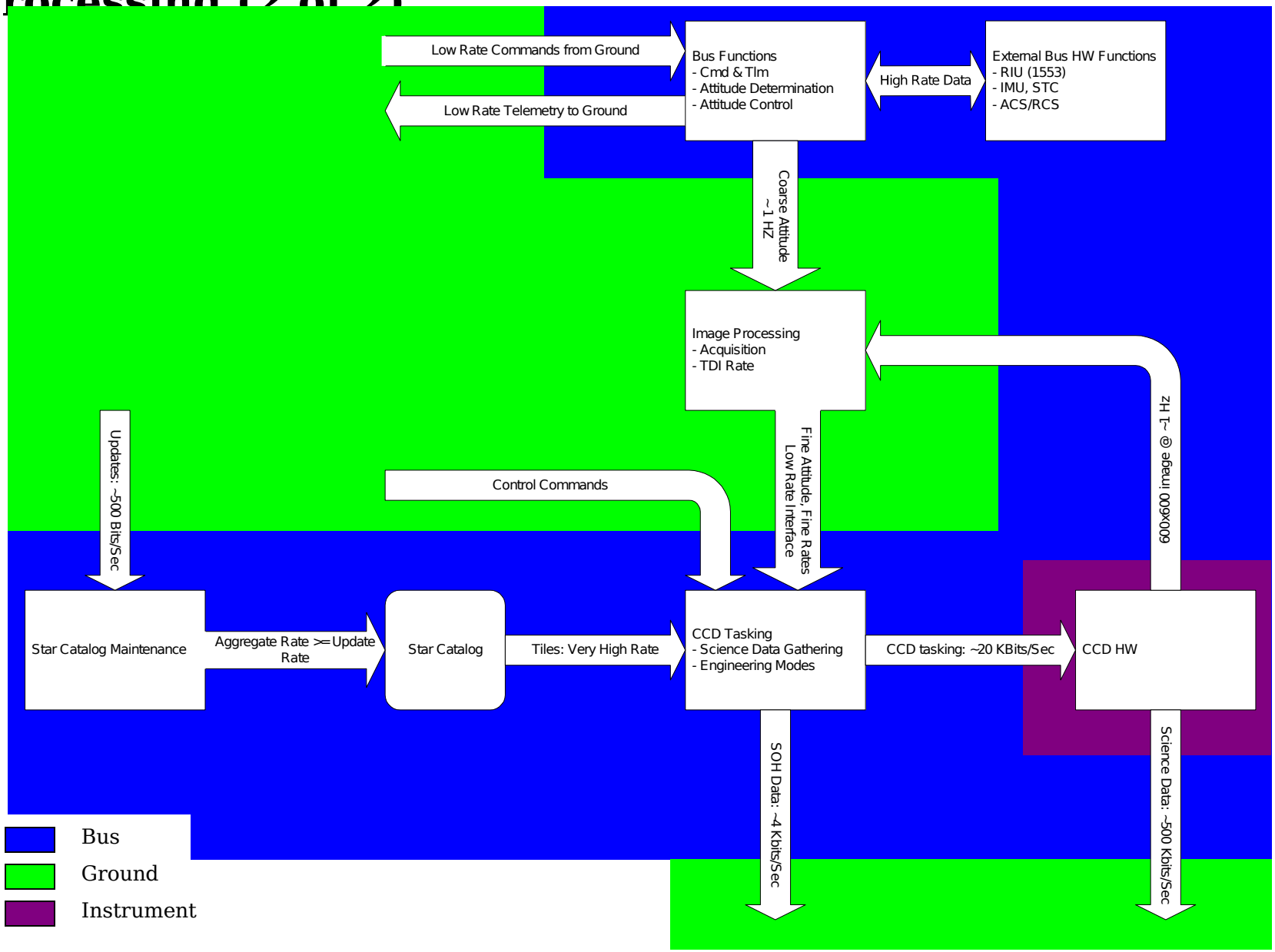


Re-allocation E: Bus Instrument Control, Ground Image Processing (1 of 2)

Re-Allocation Approach E	Baseline	Delta	Delta Cost
Processing			
Image Processing	Instrument Processor	Ground Processing	Decrease
CCD Tasking	Instrument Processor	Bus Processor	No Change
Star Catalog Maintenance	Instrument Processor	Bus Processor	No Change
Interfaces			
Coarse Attitude/Rates	Bus/Instrument	Bus/Ground (Existing)	No Change
Tracking Image	Instrument Internal	Instrument/Ground (New)	Increase
Fine Attitude/Rates	Instrument Internal	Ground/Bus (New)	Minor Increase
Star Catalog Updates	Ground/Bus/Instrument	Ground/Bus (Existing)	No Change
Instrument Control	Ground/Bus/Instrument	Ground/Bus (Existing)	No Change
CCD Tasking	Instrument Internal	Bus/Instrument (New)	No Change
Hardware (use optional hardware configuration)			
Instrument Processor	2 x RHC-3001	Not Needed	$500K Parts
Instrument 1553 I/F	2 x Harris 1553 Module	Not Needed	$200K Parts
Instrument Flash Memory	1 x 1 Gbyte (shared)	Not Needed	$100K Parts
Instrument CCD Control I/F	Instrument Internal	Not Needed	Offsetting Decrease
Bus CCD Control I/F	Not Required	Required	Offsetting Increase
Instrument Processor Related Manufacturing, Integ. & Test	Baseline	Significantly Reduced	Significant Decrease
Instrument Weight	Baseline	Reduced	Decrease
Bus Processor Design, Manufacturing, Integ. & Test	Baseline	Increased Complexity (additional HW interfaces)	Increase
Uplink Rate	2,000 bps	-	-

- Risk Increase
  - Less processing bandwidth is available (one processor for both Instrument & Bus Functions instead of 2)
  - Continuous ground processing w/low rate uplink required for science data collection (less autonomy)
- Risk Reduction
  - Less flight HW
  - Instrument/Bus 1553 I/F not required
  - Ground image processing will lessen onboard processing requirements
  - Increase in reliability (I.e. less HW)

Re-allocation E: Bus Instrument Control, Ground Image Processing (2 of 2)



Re-allocation of Instrument Flight Software Functions to Ground Processing

- Movement of software functions from flight to ground is likely to decrease the cost of software development.
  - Processing and memory constraints should no longer be a factor - less design and implement effort needed for optimizations
  - Data persistency (I.e. Star Catalog) requirements are more easily implemented
  - Ground processing design and implementation effort for a workstation target (more support tools and functions) less than the effort for an embedded target.
  - Re-use of existing “ground” (USNO) software might be possible
  - Function Criticality and test requirements will stay the same
  - Some increase in SW developments costs due to required support of additional space/ground data flow
- Re-allocation of SW development responsibilities may need to be pursued. Various approaches should be evaluated for technical and programmatic viability.

Re-allocation of Instrument Flight Software Functions to Bus Processor (1 of 2)

- Movement of all software functions from the Instrument Processor to Bus Processor may result in a reduction to the overall cost of the flight software effort. Various approaches should be evaluated for technical and programmatic viability.

- Factors independent from the allocation of FSW functions
  - Cost savings: No instrument boot and RM development
  - Cost savings: No Bus/Instrument 1553 IF development
  - Cost increase: Additional design and implementation optimization efforts may be needed due to less available processing power (1 vs 2 processors).

Re-allocation of Instrument Flight Software Functions to Bus Processor (2 of 2)

- NRL: Bus FSW functions, LM ATC: Instrument FSW Functions
  - No change: Data interface definitions (still required but are SW bus vs 1553 Bus)
  - Cost Increase: LM ATC dependent on Bus Functionality
    - Increased organization dependencies - more documentation
    - Potential decrease in productivity due to required schedule synchronization
    - Higher integration and test costs

- NRL: All Flight SW functions
  - Cost increase
    - Less instrument SW/HW team integration resulting in more formal interface documentation, and potentially less productivity due to required schedule synchronization.
    - Lack of SW team proximity to instrument design, development and test activities.
  - Cost savings
    - Increase in SW team integration - less formal interface documentation; SW schedule integration is internal vs external
    - Single development environment
    - Reduced team management overhead